Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.058”**

**G**

**SOURCE**

**.092”**

**Top Material: Al**

**Backside Material: Ti/Ni/Ag**

**Gate: .007 x .013”**

**Backside Potential: DRAIN**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .058” X .092” DATE: 11/13/20**

**MFG: ANALOG POWER THICKNESS .007” P/N: AM30P20-500**

**DG 10.1.2**

#### Rev B, 7/1